REMARKS

Applicants respectfully traverse and request reconsideration.

Applicants wish to thank the Examiner for the notice that claims 41-43 are allowed and that claims 6, 19, 32 and 44 would be allowed if written in independent form.

Claim 43 stands rejected under 35 U.S.C. § 101 because the claimed invention is allegedly directed to non-statutory subject matter. Claim 43 has been amended. Accordingly, Applicants respectfully request withdrawal of the rejection.

Claims 1-5, 7-12, 14-18, 20-31 and 33-40 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over by Donham et al. in view of Storm et al. Applicants have amended independent claims to clarify that the ALU/memory pairs are operative to perform both texture operations and color operations by the ALU, for example, being operative to read and write from its paired memory to perform both texture and color operations. Neither of the cited references teach or suggest this structure or operation. For example, the execution/math (104-105) – FIFO (106) pair of Donham alleged to correspond to the claimed ALU/memory pairs operate differently. The execution and math engines in Donham do not read from and write to the FIFO 106 to perform both texture and color operations. Instead, the FIFO 106 of Donham is shown as not being coupled to the ALUs 136a, 136b, etc. The FIFO 106 is not used by the ALU and the ALUs do not read and write to the FIFO. Instead, the FIFO 106 in Donham is merely a packet FIFO that simply stores a current packet that contains OP codes and is not connected to the math unit 105. This is stated for example, in col. 17, lns. 39-56 of Donham.

The Storm reference also fails to teach this subject matter. The office action, for example, states on page 4 that the alleged ALU/memory pair of floating blocks 152 and SRAM 153 operate as claimed. However, the detailed diagram of block 152 is shown in FIG. 6 of

Storm and as stated in col. 12, lns. 28-67 and as shown in FIG. 6, only the F-core is coupled to SRAM 153. As shown by the bus line from F-core block 352 to SRAM in FIG. 6, only the F-core block accesses the SRAM as described for example in cols. 12 and 13 of Storm. As described, the F-core block 352 uses the SRAM to store microinstructions and data for screen space conversions, for example. The shading core or lighting core block (L-core block) 354 uses a different RAM referred to as on-chip RAM and also uses a different microinstruction word length namely a 48 bit data word which is different from the F-core block which is stated as using a 36 bit microinstruction word stored in the SRAM 153. Storm like prior art systems, divides up texture and color operations among differing processors and memories. In contrast, Applicants claim, inter alia, a structure and operation wherein the same ALU is operative to read and write from the same memory to perform both texture and color operations. Since the references do not teach the claimed subject matter, Applicants respectfully submit that the remaining claims are also in condition for allowance.

The dependent claims add additional novel and non-obvious subject matter.

Applicants respectfully submit that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,
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Dated: March 10, 2010

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